3εFERRO

Energy efficient Embedded Non-volatile Memory Logic based on Ferroelectric Hf(Zr)O2

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INTRODUCTION

This document describes the overall impact of the work carried out in the 3εFERRO project. The detailed experimental, modelling simulation and design work are described in the relevant deliverables, indicated in the text. Here we focus on the probable impact to future work and indicate the specific contribution of 3εFERRO.

3εFERRO is aimed at improving the current status of embedded FeRAM by introducing new ferroelectric materials (HfO_2) and develop a competitive FeRAM which could replace eFlash in MCUs for IoT. A second major ambition is to enrich eFeRAM with novel LiM circuit designs in order to improve the energy efficiency of MCUs and increase their capabilities to process sensory data at the place where they are stored adding flexibility and increasing the range of applications. Thirdly, we have developed FeFET edge logic based on 28 nm CMOS technology from GlobalFoundries. Thus, there are three major ambitions:

- Materials optimization and solutions to specific, device determining materials problems;
- Circuit optimization and logic in memory design for low power IoT applications
- 1T-1C memory arrays and 1T FeFETs, integrated with CMOS providing the conditions for technology transfer for development of industrial products

To advance beyond the state of the art, the project faced significant technical challenges and had to attain the following four technical objectives:

- Optimization of Ferroelectric materials & interfaces
- Fine-grained LiM design & architecture
- Integration of Ferroelectric- $Hf(Zr)O_2$-based NVM arrays
- Memory test, validation and benchmarking

PROJECT IMPACT

Here we present **four key aspects** of the project work which we believe will impact future research and development as well as providing leverage for new funding requests. We conclude by summarizing some key metrics regarding our communication and dissemination of the project results.

1. Optimized BEOL-compatible ferroelectric HfO_2-based scaled FeRAM, co-integrated with 130nm CMOS for embedded NVM applications

The characterization of the final demonstrator is reported in the D5.3 and a paper will be submitted for presentation at the IEDM 2021 conference.

The optimized MAD200v3 wafers contain six 16 kbit arrays per chip (3 with Source Follower to probe internal voltages, 3 without SF; 3 corresponds to different capacitor areas). The MAD200 wafers were made using 130 nm CMOS from ST. The BEOL FeRAM and capacitor arrays have been fabricated between CEA and NaMLab, as described in D5.1. In the MAD200 wafers, the 16 kb arrays over CMOS are physically separated from the capacitor dies. The first demonstrator, reported in D5.2, used circuits optimized for OxRRAMs. The second demonstrator has adapted the sense amplifiers to the signals expected from FeRAMs and represents a major achievement of the project. We have observed

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- Scan chain, SA, write-back after read and pulse generators all work, set/reset 2 µs at V_{dd} = 4.8 V. Initial results in these conditions show zero 1T-1C bitfail.
- 1C polarization of 16k array 10 µC/cm² < $2P_R$ < 25 µC/cm² for typical capacitor sizes of 0.36 µm², 0.24 µm², 0.16 µm²
- Typical reference voltage used to characterize the bitcells is between 0.5 and 1.1 V.
- Zero bitfail to 4σ with 0.2 V memory window after 1000 cycles.

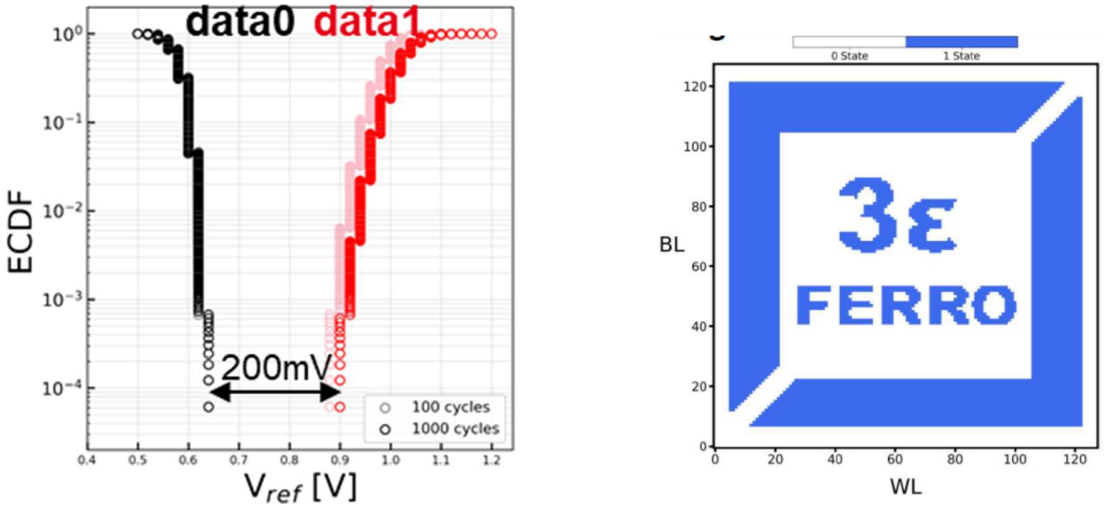

Figure 1 Initial characterization of 16k FeRAM array on MD200v3 lot showing (left) the memory window to 4s and (right) the zero bitfail after 1000 cycles performed on the word vs. bitline 128 × 128 memory array storing the 3εFERRO logo (to be published).

Given these very encouraging results, the next steps concern statistically significant reliability analysis, specifically on retention, endurance, and solder reflow.

Retention on single devices

Thermally activated degradation, imprint, domain pinning all contribute to retention kinetics. It is therefore necessary to characterize all combinations of ferroelectric states of a memory cell before and after retention bake, i.e. same state (positive or negative), new same state (positive or negative after switch back and forth), opposite state (positive or negative after switch). This methodology was first developed by Texas instruments [Rodriguez Trans Device Mater. Reliability 4 (2004)].

As can be seen from the schematic, four capacitors undergoing different pulse sequences are necessary for a complete retention test on a single “device”. The tests are performed for different times at a variety of temperatures, in order to extract activation energies. Precision is attained by measuring several capacitors for each condition to minimize variability.

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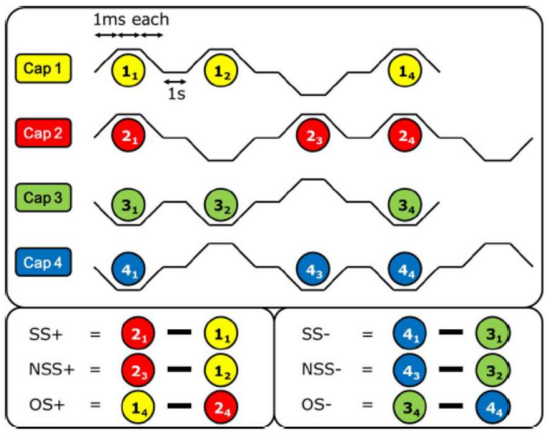

Figure 2 Methodology first developed by Texas instruments for endurance/retention tests of ferroelectric capacitors, considering the polarization state and switching history [Rodriguez Trans Device Mater. Reliability 4, (2004)].

Initial retention analysis has been done at NaMLab at 85, 120 and 155 °C on wafers 18 & 19 (Si:HfO_2) using the equation as proposed by Texas Instruments for PZT ferroelectric material:

$$P(t,T) = P_0 - \Delta P(T) - m(T)\log(t)$$

Where the second term is the thermally induced change in polarization after one hour annealing at a temperature T and m(T), the subsequent rate of change of polarization at constant temperature. This yielded two distinct activation energies, 0.25 and 1.5 eV for retention degradation similar to PZT. Accordingly, general mechanisms for retention degradation are similar in doped HfO_2 based capacitors and in the PZT case. Just the magnitude of the process is higher for analyzed Si-doped HfO_2 based capacitors.

FRAMs are attractive in terms of scalability potential, possibility of 3D integration, power consumption, read and write speed, integration cost (number of additional steps) and cycling endurance (10^{11}), thus justifying ST investment in 3εFERRO.

However, there are outstanding questions before an informed decision on exploiting this memory technology can be taken. The main question is the data retention at temperature, 85°C for IoT consumer electronics, 125°C for industrial applications, 165°C for automotive applications. Two other outstanding problems to be addressed are the achievable solder reflow specifications and the endurance figures with sufficient statistics.

Retention measurements on 16kb memory arrays

Based on the first retention results yielded by the project, the following practical characterization steps appear necessary

- Full retention analysis @ 85, 125 and 165 °C
- Solder reflow 3 x 10 minutes @ 260°C in N_2 atmosphere
- Endurance to 10^{11} cycles @ 85, 125 and 165°C

All experiments should be done on test chips (16 kb) in order to acquire sufficient statistics for more reliable extrapolation but also on individual, larger capacitors for analysis of physical/chemical properties

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(defects, domain switching, redox reactions) to be correlated with the statistically reliable electrical characterizations. Experiments on films w/o top electrode can be done in N_2 and/or UHV.

Retention analysis will be done for at least four temperatures after typically 1000 hr bake (~10^6 sec) and combining fresh/cycled, erased/written devices under test. The combination of four temperatures and the time evolution will provide the data to extract the activation energies defining the retention behaviour. Physical modelling is necessary to quantify the activation energy or, in the case of more than one mechanism for retention/endurance limitation, e.g. temperature threshold for electrode/ferroelectric interdiffusion, the activation energies and therefore understand the physical mechanism(-s) of retention degradation. Breakdown measurement (time/voltage to failure) are also to be done.

Together with the recently reported results by Sony on 8 nm thick $HfZrO_2$ in a 64 kb 1T-1C array the 16 kb test vehicle results of 3εFERRO represent the state of the art for characterizing hafnia based ferroelectric capacitors for BEoL applications and allow extrapolation. However, it is clearly two orders of magnitude below the statistics required of raw data for industrial qualification. The objective is to attain a defect density < 10^{-7}, i.e. less than one capacitor fail per 10 Mb. To do so, we plan to upgrade from 16 kb to 1 Mb. This can be implemented in the MAD200 whose process flow is already controlled.

The pulse generators of the 16kb FRAM allow reaching read/write times of 20 ns, corresponding to the "mission profiles" of ST.

The same pulse generators can provide 2.5-2.0 V, however, film optimization and capacitor engineering is still required in order to reduce the coercive field while maintaining a high remanent polarization. Currently, this has been demonstrated by Sony using 8 nm HZO (2.0 V coercive voltage) at IMW2021 (J. Okuno, IMW 2021). The present results on the film optimization reported in D2.3 are in this respect encouraging suggesting that even 6 nm may be attainable with ~1.5 V operating voltage.

Solder reflow

Solder reflow is essential for packaging products. The encouraging reliability results for FeRAMs reported in the project call for urgent solder reflow tests. The solder reflow capability of the ferroelectric hafnium oxide used in FeFETs was proven already in [S. Dünkel et al., *A FeFET based super-low-power ultra-fast embedded NVM technology for 22nm FDSOI and beyond*, 2017 IEEE International Electron Devices Meeting (IEDM), San Francisco, CA, 2017, pp. 19.7.1-19.7.4.]. However, for the BEOL capacitor devices these findings have to be proven by experiments, since the different material stack and integration flow might have an impact on high-temperature retention First results on Si:HfO2 based 16k FeRAM array of 3 x 50 seconds solder reflow at 250°C show that the main ferroelectric characteristics are maintained.

Materials characterization

The project has also had considerable impact on basic materials research and optimization of hafnia-based ferroelectrics. The article by Hamouda et al on the physical chemistry of the TiN/HZO interface [W. Hamouda, A. Pancotti, C. Lubin, L. Tortech, C. Richter, T. Mikolajick, U. Schroeder and N. Barrett, J. Appl. Phys. 127, 064105 (2020)] was the most downloaded manuscript in 2020 in the Dielectrics, Ferroelectrics and Multiferroics section of the Journal of Applied Physics (2400 downloads), most probably because it provided a direct measurement of the oxygen vacancy concentration profile over the first few nm in the HZO.

2. Logic in Memory FeFET applications

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The design and characterization for FeFET LiM applications are reported in detail in D4.4.

The ferroelectric field effect transistor (FeFET) intrinsically provides computational as well as memory capabilities. Moreover, the availability of industry-scale integrated FeFETs together with standard CMOS-transistors as offered by GLOBALFOUNDRIES for the 3εFERRO project has paved the way for the development of versatile circuit approaches. A 9mm^2 3εFerro contribution on the MPW0359 tape-out in March 2020 contains test structures for various TCAM and reconfigurable non-volatile logic cells, adders and multipliers (where reconfigurable parameter sets can be stored in FeFETs), as well as more complex hardware accelerators such as a dedicated image filter and a two-layer convolutional neural network. First functional hardware has been available since January 2021. The electrical characterization results, together with simulation results from a benchmarking platform, reveal detailed information especially for use cases of FeFETs in logic circuits that go well beyond their application in pure memory arrays. Publication of these results is envisaged for second half of 2021.

For the FeFET LiM circuit designs in the 3εFERRO project the actual performance characteristics of the FeFET devices based on the 28nm SLP CMOS technology at GLOBALFOUNDRIES have to be taken into account. The further device development in this technology is not part of the 3εFERRO project. The most important performance characteristics of the FeFETs can be summarized as follows:

- Non-destructive read-out
- Size equal to / smaller then smallest embedded NVM competitors cells < 0.03 µm^2
- Low energy to switch 1-10 pJ/bit
- Access time 5 ns
- Extrapolated Retention: 10 years
- Field cycling endurance with reasonable memory window: 10^5 cycles
- Soldering reflow possible with no impact on FeFET performance: 260°C 50 minutes

In order to design functional systems, the individual performance characteristics (as e.g. described above) have to be taken into account. That is, the FeFET can be fully integrated into CMOS, exhibits data retention > 10 years and features access times for read operation in the sub-10ns and write operation of < 10 ns up to microsecond range, depending on the specific design constraints. Read endurance is virtually unlimited, while write endurance is limited to ~10^5 switching cycles. Thus, the integration of FeFETs into novel LiM applications makes most sense where e.g. an internal value, saved in the ferroelectric layer of the FeFET (e.g. a filter kernel) that has to be changed not very frequently (e.g. ~ms-range), is processed in connection with an externally applied input data stream. To demonstrate the FeFETs performance for application in LiM designs, in Task 4.3 we have realized a real-time image filter circuit demonstrator. In this application the filter kernel can be reconfigured to hold e.g. edge detection as well as sharpening or blurring filters, depending on the stored values.

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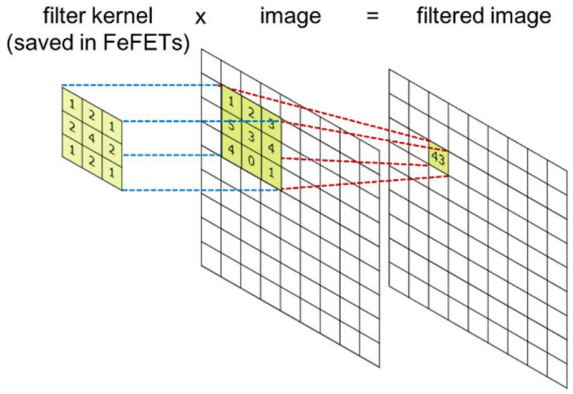

Figure 3 Schematic of image application showing the filter kernel convolution with the input image to produce a real-time filtered result.

NaMLab owns the basic IP on HfO_2-based FE devices (US 7,709,359; US 8,304,823) and founded a spin-off (Ferroelectric Memory Company, FMC) to specifically exploit the FeFET IP. Circuits, designs and modelling results developed in the project can be useful for other nano-electronic architectures resulting in future collaborations with industry. The main interest is currently from GlobalFoundries and their production partners. The exploitation of 1T FeFET LiM results is envisaged by extending the roadmap of NaMLab spin-off FMC beyond pure memory block IP towards fine-grain LiM implementations. 3εFERRO has provided leverage for several collaborative projects underway or being prepared. SPICE models of FeFETs are reused for the design of neuromorphic circuits in the H2020 BeFerroSynaptic project. Moreover, the FeCAP SPICE model was extended by a polarization dependent leakage term that is used to model the electrical behavior of ferroelectric tunneling junctions (FTJ) in the H2020 BeFerroSynaptic project as well as in the DFG (German Science Foundation) funded project ReLoFeMris, both being coordinated by NaMLab.

After demonstration of the FeFET-based image filter concept in the 3εFerro project, a natural next step would be the upscaling of the image filter and CNN macros (to enable more powerful low-power embedded image-processing and AI accelerators) as well as the downscaling of the used FeFETs (both in existing 28 nm technology and in more aggressive nodes) to enable more powerful and lean designs. This work could be undertaken in a successor project with the potential participation of GLOBALFOUNDRIES, currently under discussion. Other design approaches of interest include TCAM circuits (for Hamming distance estimation in machine learning) and non-volatile fine-grain reconfigurable computing resources.

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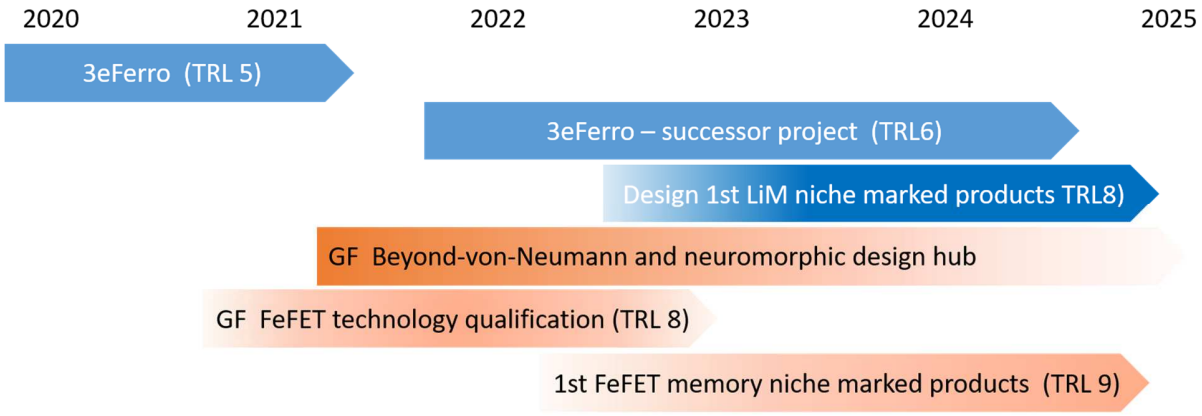

Figure 4 Updated FeFET post project roadmap for CiM and LiM designs showing how current GF technology and future innovative technologies might run in parallel.

A "Beyond-von-Neumann and neuromorphic design hub" for GLOBALFOUNDRIES' FeFET technology exploitation is also under discussion and might be initiated already in the second half of 2021. Besides the work on FeFET-based CiM and LiM concepts performed in the 3εFerro project there is a fast-growing worldwide interest in this topic within the academic and industrial design community. As indicated by the comparatively large number of citations, several other research groups were inspired by the work performed in 3εFERRO and might become potential research partners, e.g.: [T. Soliman *et al.*, "Ultra-Low Power Flexible Precision FeFET Based Analog In-Memory Computing," *2020 IEEE International Electron Devices Meeting (IEDM)*, 2020, pp. 29.2.1-29.2.4, doi: 10.1109/IEDM13553.2020.9372124][Kazemi, Arman, et al. "In-Memory Nearest Neighbor Search with FeFET Multi-Bit Content-Addressable Memories." *arXiv preprint arXiv:2011.07095* (2020)][S. Dutta et al., "Experimental Demonstration of Gate-Level Logic Camouflaging and Run-Time Reconfigurability Using Ferroelectric FET for Hardware Security," in IEEE Transactions on Electron Devices, vol. 68, no. 2, pp. 516-522, Feb. 2021, doi: 10.1109/TED.2020.3045380.], just to name some examples. We can already affirm that early publications from the 3εFerro project [O'Connor et al IEEE 2019 10.1109/VLSI-SoC.2018.8644809, Beyer et al. 2020 IEEE International Memory Workshop (IMW), 2020, pp. 1-4, doi: 10.1109/IMW48823.2020.9108150], undoubtedly helped to boost the interest in FeFET-based beyond-von-Neumann concepts.

Finally, depending on progress in the FeFET technology qualification at GLOBALFOUNDRIES the design of first niche market products might be envisaged to start in 2022.

3. LiM, CiM roadmap using 1T-1C and 1T technologies

The project design work for LiM and CiM is reported in D4.3 and D4.4.

Exploratory circuits were designed at the cell level in order to gain further understanding of the benefits and limitations of the BEOL ferroelectric capacitor technology, in particular, leveraging the additional degree of freedom in terms of size of ferroelectric capacitor (as opposed to the FeFET technology, where the size of the ferroelectric layer is linked to the size of the transistor). Variants of three test structures were designed: pseudo-FeFET, 2TnC, TCAM. All circuits were taped-out in June 2019 to CMP using ST HCMOS9 130nm technology with FeRAM integrated by CEA-LETI in BEOL. Bare CMOS dies have been received BEOL FeRAM devices were then added. First test results demonstrate the functionality of the

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circuits (on MAD200 Wafer D20S0237A w23), and are particularly promising for the 2T1C and 2TnC structures. The transistor threshold voltages are not affected by program/erase operations and multiple states have been programmed to the capacitor. Switching kinetics for program/erase also look reasonable with expected voltage/time tradeoff. Further measurements such as endurance, retention, wafer mapping, capacitor-size dependency etc. are to be carried out imminently. Publication of these results is envisaged for second half of 2021.

Exploratory non-volatile circuits also benefit from the use of FeFET devices in other circuit-level design approaches (non-volatile logic, Lookup Tables, routing structures and TCAM) for additional functionality. All circuits were taped-out at the end of March 2020 to GLOBALFOUNDRIES Fab1 LLC & Co. KG, Dresden, Germany on MPW0359 and were finally received in January 2021. First test results demonstrate the functionality of the circuits, in particular for the structures combining ternary content addressable memory and normal memory capability: the TC-MEM. A 1-bit TC-MEM circuit is functional and exhibits measurement results which agree with simulations. Such a circuit can easily be scaled to multi-bit circuits and work has started on exploring their use in implementing reversible functions (targeting cryptography applications) using a single memory table instead of two, as well as for in-memory-computing concepts (targeting AI applications).

Both FRAM and FeFET LiM, CiM circuits are now under extensive tests which will be continued after the end of the project.

Finally, a benchmarking platform based on circuit-level Pareto-Front generation and system-level evaluation was developed, to make extensive evaluations of multiple device, circuit, architecture and benchmark scenarios and fully explore the possibilities of FeRAM-based circuits and LiM architectures in a cost-effective manner and project device characteristics onto meaningful system-level performance metrics. We are currently assessing how to best exploit the platform in a possible Design Technology Co-optimization system and exploring potential commercialization.

4. Negative Capacitance (NC) proof of principle

The full assessment of the project work is reported in D2.4 and D4.5, which are merged into a single deliverable.

Early in the project (2018-19) we realized that the NCFET demonstrator was too ambitious with respect to the state of the art and the probable advances in knowledge during the project. The evolution of the state of the art in the field within the period of 2017-2020 confirms our conclusion, as clearly reflected by NCFET papers in IEDM conferences:

-IEDM 2017- special session on NC FET with focus on steep-slope devices
-IEDM 2018- similar to 2017
-IEDM 2019- special session on NC devices, mainly fundamental aspects are addressed
-IEDM 2020- no special session on NC, very few papers mention NC effect

The trend suggests that it was gradually becoming clear for the community that the technology is not mature enough and more efforts need to be focused on understanding the underlying physics and materials aspects. In this context, our decision taken as early as 2018 to scale back the NC demonstrator to proof of principle looks fully justified and timely.

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The major problem faced by research into NC is that the theoretical models used do not correctly explain or predict the experimental results. This is probably because they were often simple, single domain models and did not take into account sufficiently the formation of ferroelectric domains, domain switching dynamics and charge trapping. Much theoretical work uses phenomenological models and there is a clear need for more fundamental modelling using first principles calculations.

One difficulty we recognized during the project was the extent to which negative capacitance appears dependent on the precise experimental conditions. Thus, NC is reported within µs-ns range but hysteresis rapidly appears as frequency decreases due to either partial switching and/or trapped charge accumulation at the interfaces. NC also appears to be voltage dependent. We have reported stable NC using a ferroelectric/dielectric layer structure, although the operational voltages are still too high for applications [Stolitchnov Appl. Phys. Lett. 117, 172902 (2020), Gastaldi, IEDM 2019]. The expected technological impact of NC research is therefore less immediate than expected at the beginning of the project. The outstanding challenges for NCFETs remain essentially the same:

- Sub threshold swing
- Hysteresis free characteristics
- Characteristics independent of measurement conditions
- Stability of characteristics with respect to the number of cycles

Progress on these four aspects requires a better understanding of switching mechanisms, the role of multi-domain formation, point defects such as oxygen vacancies and charge trapping/de-trapping. The most recent publication from the EPFL partner [Stolitchnov Appl. Phys. Lett. 117, 172902 (2020)] is one example of the research direction to be followed post-project. The return to fundamental materials understanding has also been suggested in a recent comment in Nature Electronics [Hoffmann et al. https://doi.org/10.1038/s41928-020-00474-9] to which project participants have contributed.

Such research would help to reach operational voltages 1-2 V needed for low power electronics, understand how to downscale further film thicknesses, possibly using Ge channels in NCFETs in order to minimize the interface layer. Ge FeFETs could also be more suitable as memory elements rather than NCFETs provided that, in the future, interface defect states will be adequately passivated without harming ferroelectricity in the HZO. NCSRD continues research on Ge/HZO interface in the context of FTJ memory elements for memristive devices in the framework of H21020 ICT project BeFerroSynaptic where the challenge of interface defect state passivation is addressed. We believe that the project work has contributed to a valuable reorientation of research into negative capacitance.

Communication and dissemination activities:

Key figures*: (since the beginning of the project)*

10 posters

43 oral presentations

24 invited talks

28 peer-reviewed publications

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3 workshops organized

12 PhD theses directly linked to 3eFERRO (funded by the project or by partner organizations). Two have been defended (J. Bouaziz and M. Cavallieri), the other defences will be end of 2021 or 2022. Most of the thesis defences have been delayed a few months due to the Covid-19 crisis, however, the project has clearly been beneficial to these young researchers giving them first-hand experience of a wide technological range of research activities.

1 Ferro base school for doctoral students organized (but will be held after the end of the project due to Covid restrictions

ECL and NCSRD organized the Symposium Q on Polar Oxides at EMRS Spring Meeting – 29&30 May, 2019 - with 3εFERRO financial support (1,000€). 55 abstracts were submitted and, in the framework of 3εFERRO, a half-day session was especially dedicated to ferroelectric HfO_2 growth and characterization with an invited presentation by Prof. Beatriz Noheda (Groningen University, The Netherland). Three PhD students (from ECL, NCSRD and CEA) involved in 3εFERRO made also oral presentation (each presentation included two institutions of the project), given them the possibility to present their results in front of the oxide community. About 40-45 persons attended the symposium.

3εFERRO has sponsored and co-organized the high-k workshops online in 2020 and 2021. The 2020 edition focused on the student presentations (14 presentations over 5 separate sessions). The 2021 edition followed more closely the high k workshop format in six 1hr30min sessions from 23rd April to 28th May and 11 invited speakers (total 19 presentations in 6 separate sessions): Alex Hsain (NC State), Alfred Kersch (Univ Applied Sciences Munich), Beatriz Noheda (University of Gröningen), Sayeef Salahuddin (University of California, Berkeley), Min Hyuk Park (Pusan National University), P. Buragohain (University of Nebraska), U. Böttger (RWTH Aachen), Anna Chernikova (MIPT), Cheol Seong Hwang (Seoul National University), Franz Müller (FhG IPMS-CNT Dresden), Sourav Datta (Notre Dame, IN). Overall, in average more than 80 participants attended the workshop.

Four 3εFERRO newsletters have been published (December 2018, August 2019, August 2020 and January 2021) A fifth and final newsletter is under preparation and will be published to coincide with the final project meeting in September 2021. In addition to the project website (https://3eferro.eu/images/pdf/Newsletter_2_050819.pdf), partners have also published the newsletter on their institutional sites:

- http://iramis-i.cea.fr/spec/Phocea/Vie_des_labos/News/index.php?id_news=7684
- https://infim.ro/en/project/3eferro/
- http://www.namlab.de/research/projects/projects-1

- A three minute professional video has been made (with the minimento company) summarizing the project context, challenges and work, addressing a wider public. The video has had over 1000 views and is available on YouTube as well as via partner institutional websites.

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