3εFERRO

Energy efficient Embedded Non-volatile Memory Logic based on Ferroelectric Hf(Zr)O2

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Benchmarking of ferroelectric memories with respect to other new memory technologies

The challenges linked to the miniaturization of floating gates memories, the widening of the market segment inside the electronic memory field due to the IoT, the growing appeal for more demanding automotive applications, as well as all of the intermediate "consumer" and "industrial" identified markets, have led to the rise of the eNVM " Emerging" Memories over the last ten years.

Many industrial actors are nowadays engaged in the development, industrialization and even commercialization of various solutions, the more common being

- MRAM for low temperature and High speed applications
- RRAM for low power and low cost applications
- FG gate and / or PCM for automotive applications

In addition to these solutions, since 2011 ferroelectric HfO_2 based memories have also generated considerable interest thanks to characteristics such as ease of integration and cost but also for their intrinsic interest for low energy memory operations. Indeed, the mechanisms involved appear well adapted for low power and high switching speed systems as shown in table 1. The potential of ferroelectric memory and logic technologies (FeRAMs and FeFETs) is at the heart of 3εFERRO.

Reliable data retention is one of the critical parameters to define the approachable markets and differs widely between different memory types. For the ferroelectric memories, if the theoretical temperature stability of the polarization field appears promising, it appears that many phenomena need be taken in consideration to address this topic , such as imprint , trapping and de-trapping versus time and cycle duty.

Thus, ferroelectric memory solutions are of interest for applications for very low power/low cost but they have yet to prove their interest in the reliability region, where they have to show memories windows supporting cycling, time and temperatures mission profiles.

Recently, papers have started to show improved performances for ferroelectric memories including first results for critical characteristics such as data retention, justifying a careful benchmarking of the state of the art. On the one hand, reliability must be compared with that of other emerging NVM technologies while on the other hand, we require careful assessment of the best reported metrics for hafnia based NVMs from competitors.

Sony associated with NaMLab showed at the 2020 edition of the VLSI conference a 130nm integrated test chip with BEoL ferroelectric capacitor at 64 Kbits density. Promising memory/distributions and performance plots show a full functionality with high operation speed. They also present good cycling characteristics with endurance > 10^{11} cycles and data retention of 10 years at 85°C.

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Lin and al (IEDM 2019) also presented interesting properties for 3D Capacitor based memories with HZO materials demonstrating endurance in the 10^9 cycles and data retention in the 85 to 105 °C range.

Jiang and all (IMW2020) demonstrated tight polarization distributions and very interesting temperature stability for $HfZrO_2$ stacks switching up to 700K, very promising to increase the temperature range for application (despite being at elementary test pattern level) .

Within the framework of 3εFERRO, we have compiled two benchmarking tables for FRAM (1T-1C), which have been regularly updated from M24 onwards.

Table 1 benchmarks the overall performance of the HfO_2 based FeRAM with respect to other NVMs. Table 2 compares the results obtained in 3εFERRO with the performances obtained by different authors with ferroelectric hafnia-based solution.

One can note that the items linked to performances (programing bias, time, power) are already very promising and could lead to features superior to our current reference, especially in term of power, The low bias in an acceptable range for design perspective (compatible with standard MOS feature of mother technology) and high programming speed are attainable. For the size of the memory, one must note that the main published test chip results are realized in big technology node (130 nm mainly), limiting the bit cell size. The intrinsic capacitance variations linked to the ferroelectric switch in the 1T-1C type reading scheme, that can be related to DRAM like architecture (with sensing abilities in the range of 5 to 10 fF/cell), should allow for elementary capacitor size lower than 0.035 µm² in planar configuration. This can be much lower if 3D capacitor architecture is introduced, allowing these approaches to be competitive even for advanced nodes.

One general remark on data published on 1T-1C (or FeFET) memories is the limited data retention (and data retention post cycling) characteristics. However, significant progress has been made in this respect, reported in detail in D5.3 and, at least at 85°C, retention is improving. The first positive solder reflow data, also in D5.3, are very encouraging with respect to reliability/applications. The relatively good performance seen @ 85°C can confirm that these memories will be interesting for low temperature applications (consumer electronics, IoT applications).

Thus, the most recent data from 3εFERRO with polarization evolution with different temperature represent a very interesting step towards a clearer view of the possible devices application.

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	FLASH	MRAM	PCM	RRAM	FeRAM (PZT)	FeRAM (HfO_2)	FeFET (HfO_2)
Programming power	~200pJ/bit	~20pJ/bit	~300pJ/bit	~100pJ/bit	~10fJ/bit	**~10fJ/bit**	~10fJ/bit
Write speed	20 µs	20 ns	10-100 ns	10-100 ns	<100ns	**14ns @ 2.5V**	1 µs
Endurance	10^5 - 10^6	10^6-10^{15}	10^8	10^5 - 10^6	> 10^{15}	**> 10^{11}**	10^5 - 10^6
Retention	> 125°C	85°C - 215 °C	165°C	> 125°C	125°C	**85°C**	125°C
Extra masks	Very high (>10)	Limited (3-5)	Limited (3-5)	Low (2)	Low (2)	**Low (2)**	Low (2)
Process flow	Complex	Medium	Medium	Simple	Simple	**Simple**	Simple
Scalability	Bad	Medium	High	High	Poor	**Medium (2D) High (3D)**	Medium for memory applications

Table 1. Benchmarking of overall ferroelectric FeRAM performance with respect to other NVM emerging technologies

FeRAM characteristics	[1] single device	[2] 64 kbit 1T-1C arrays	[3] 64 kbit 1T-1C arrays	[4] 16 kbit 1T-1C arrays
FE material / electrodes /integration	FE: 10nm HZO Electrodes: TiN PEALD BEOL	FE: 10nm HZO Electrodes: TiN PVD MEOL	FE: 8nm HZO Electrodes: TiN PVD MEOL	FE: 10nm HZO, HZO:La, HfO_2:Si Electrodes: TiN PVD BEOL
Capacitor area	NA (2D and 3D)	1µm² - 0.4 µm²	1µm² - 0.06 µm²	0.36 µm² - 0.053 µm²
Operating speed	~ µs	Down to 14 ns at 2.5 V	Down to 16 ns at 2.0 V	Down to 4 ns at 4.8 V
Operating voltage	2.5 V	Down to 2.5 V	Down to 2.0 V	Down to 2.5 V
Endurance	10^{10} cycles (2D) 10^9 cycles (3D)	> 10^{11} (projected at 10 MHz on single capacitors)	> 10^9 (measured at 100 kHz on single capacitors) 10^8 cycles measured at 3.5 V 100 ns 85°C on 4kbit with no bitfail $3x10^{18}$ cycles *extrapolated* at 2V at 1ppm	10^{11} measured on HZO single capa > 10^{13} extrapolated @ 2.5 MV/cm, HZO single capa NA on arrays
Retention	$5x10^4$ s @ 105°C (60% loss)	85°C > 6000 s	85°C > 6000 s	OS 120°C $4x10^5$ s
Solder reflow compatibility	NA	NA	NA	Yes
Technology node (wafer)	180nm or 130nm (200mm)	130nm (200mm)	130nm (200mm)	130nm (200mm)

[1] ITRI, Taiwan, IEDM 2019 [2] SONY/NaMlab, VLSI 2020 [3] SONY/NaMlab, IMW 2021 [4] 3eFERRO consortium

Table 2. Benchmark of 3εFERRO FeRAM performances compared with state of the art published results from competitors.

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